Replace the paragraph beginning on page 1, line 10 with the following paragraph:

B2

"The present invention relates to a field effect transistor (FET) which is formed in a silicon layer located on an insulating film, or a silicon on insulator (SOI) substrate. The SOI substrate has an insulating film and a thin silicon layer formed over a conductive substrate used as the conventional substrate to form the FET. The present invention also relates to a method of manufacturing such a field effect transistor."

Replace the paragraph beginning on page 4, line 13 with the following paragraph:

B3

"According to the present invention, the field effect transistor is capable of restraining the reduction of the drive current thereof. The transistor of the present invention can be formed in a microscopic size."

Replace the paragraph beginning on page 6, line 12 with the following paragraph:

B4

"Fig. 1 is a cross-sectional view describing a field effect transistor according to a first preferred embodiment, showing in detail a fully depleted SOI-FET formed on an SOI substrate. The SOI-FET is formed in a thin silicon film (SOI layer) which is formed on an insulating film of the SOI substrate."

Replace the paragraph beginning on page 11, line 11 with the following paragraph:

B5

"In fact, it will be expected that the contact specific resistance would be further reduced, by considering the accumulation resistance Rac, the spreading resistance Rsp and the sheet resistance Rsh-s in the above formula. The contact specific resistance between the cobalt silicide (CoSix) and the silicon of the first preferred embodiment is far smaller than $1x10^{-7}$ Ω-cm^2 introduced in the above second thesis."

Replace the paragraph beginning on page 11, line 16 with the following paragraph:

B6

"Fig. 4 is an explanation diagram showing the drain voltage dependence of a threshold voltage for the fully depleted SOI-FET. In Fig. 4, the SOI-FET is the N type MOS transistor, as well as Fig. 3(a) and Fig. 3(b). The drain voltage of the conventional SOI-FET is shown as a mark of "X" and that of the first preferred embodiment is shown as a mark of "●". When a substrate floating effect, such as a parasitic bipolar effect occurs in the fully depleted SOI-FET, the drain voltage will rise up. Fig. 4 shows that a reduction of a threshold voltage of the conventional SOI-FET is remarkable, as a drain voltage rises up. However, the reduction of the threshold voltage of the SOI-FET of the first preferred embodiment is minimal. In other words, a leakage current of the SOI-FET can be cut down."

Replace the paragraph beginning on page 12, line 8 with the following paragraph:

"According to the first preferred embodiment of the present invention, a field effect transistor capable of restraining the reduction of the drive current of the SOI-FET is provided. Further, the SOI-FET of the first preferred embodiment enables formation of microscopic devices. Additionally, since the SOI-FET of the first preferred embodiment can precisely reduce the leakage current, the SOI-FET is useful as a low-power transistor."

Replace the paragraph beginning on page 13, line 8 with the following paragraph:

"The source and the drain regions include the highly doped silicon layers 18a and 18b and metallic silicide layers 19a and 19b, respectively. The metallic silicide layers 19a and 19b are composed of refractory metal and silicon. An amount of refractory metal contained in the metallic silicide layers 19a and 19b is more than that of silicon. In the second embodiment as well as the first embodiment, the metallic silicide layers 19a and 19b are comprised of a CoSiz layer having a ratio of cobalt to silicon that is one to z ($1<z<2$). The CoSiz layers 19a and 19b are formed by the conventional silicide process. In more detail, the source region and the drain region except under the sidewalls 7a and 7b are changed into the cobalt silicide layers 19a and 19b."

Replace the paragraph beginning on page 13, line 17 with the following paragraph:

B9

"The CoSiz layers 19a and 19b respectively have a thickness which is equal to or more than 80% thickness of from top surfaces of the CoSiz layers 19a and 19b to bottom surfaces of the SOI layer 3. In other words, portions 21a and 21b of the highly doped silicon layers 18a and 18b respectively extend between bottom surfaces of the CoSiz layers 19a and 19b and a top surface of the insulating layer 2."

Replace the paragraph beginning on page 14, line 5 with the following paragraph:

B10

"If a conventional $CoSi_2$ layer is used as the metallic silicide layer, the conventional $CoSi_2$ layer would be formed so as to have a thickness of the $CoSi_2$ layer less than 80% thickness of from top surfaces of the $CoSi_2$ to bottom surfaces of the SOI layer."

Replace the paragraph beginning on page 14, line 8 with the following paragraph:

B11

"On the other hand, 1993 IEEE, pp. IEDM 93-723 ~ 726-IEDM 93, "OPTIMIZATION OF SERIES RESISTANCE IN SUB-0.2 m SOI MOSFETs" (hereinafter a third thesis), reports the following concerning a conventional $CoSi_2$ layer:"

Replace the paragraph beginning on page 15, line 9 with the following paragraph:

"A method of manufacturing the field effect transistor described in the third preferred embodiment, will be shown hereinafter referring to Fig. 5(a) – Fig. 5(c). In Fig. 5(a), the SOI-FET is formed on an SOI substrate, which comprises a silicon substrate 51, an insulating film 52, and an SOI layer 53. Field oxide films 56a and 56b and heavily doped impurity layers 58a and 58b are formed in the SOI layer 53 by using a conventional process. A channel region is defined between the pair of highly doped silicon layers 58a and 58b. A gate electrode 55 is formed on a gate oxide film 54 and located on the channel region. Cobalt (Co) film 60 is formed on the gate electrode 55 and highly doped silicon layers 58a and 58b. The cobalt film 60 is a refractory metal film for forming a metallic silicide layer. A titanium (Ti) film 61 or a titanium nitride (TiN) film 61 are formed on the cobalt film 60 as an antioxidant film 61 when a following heat treatment."

Replace the paragraph beginning on page 17, line 12 with the following paragraph:

"According to the present invention, a field effect transistor capable of restraining the reduction of the current drive capacity of the transistor is provided. Also, the transistor as provided enables formation of microscopic devices including the SOI-FET described above. Since the transistor of the present invention can precisely reduce the